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| 10/040,920 | 12/28/2001 | Juan G. Revilla | 10559-566001 P12728 | 3816 |

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| EXAMINER | |
|---|---|
| THAI, TUAN V | |

| ART UNIT | PAPER NUMBER |
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| 2186 | |

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/040,920 | REVILLA ET AL. | |
| | Examiner | Art Unit | |
| | Tuan V. Thai | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

**Part III DETAILED ACTION**

***Specification***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 27, 2004 has been entered. Claims 1-31 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

***Claim Rejections - 35 USC § 112***

3. Claims 11-14 and 34 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 11, the following terms/recitations lack proper antecedent basis: "the state" (line 6). Claims 12-14 and 34 are also rejected since they are dependent upon the rejected claim 11.

*Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-6, 11-13, 15-16, 32 and 40 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lyon (USPN: 6,470,437);

As per claim 1; Lyon discloses the invention as claimed including a method comprises receiving a request (cache access) for access to a memory location by presenting a virtual tag to CAM (e.g. see column 2, lines 49-50; column 5, line 44); identifying a memory block including the memory location (e.g. see column 2, lines 50-52); Lyon further discloses examining a local memory descriptor (TLB HIT bit) associated with the memory block (TLB RAM memory block) and accessing a local addressable memory (TLB) in response to the TLB hit bit to retrieve physical tag from TLB RAM, the TLB hit bits are then compared to cache tag to determined cache hit or cache miss (e.g. see column 2, line 63

bridging column 3, line 1; also see column 2, lines 52-56); Lyon further discloses the local addressable memory (TLB) is within the cache which is at the same level of memory as the cache as being claimed (e.g. see figure 3, column 5, lines 28 et seq.);

As per claim 2, Lyon discloses in response to TLB hit or the memory location existing in the local addressable memory (TLB), accessing the memory location, for example, a physical tag is then retrieved from the TLB RAM 118 (e.g. see column 5, lines 10-13);

As per claim 3, generating an illegal access violation exception in response to the memory location not existing in the local addressable memory (TLB) is equivalently taught by Lyon as when there is a TLB MISS condition (memory location is not in the TLB), the virtual hit vector 214 generates all binary "0s" (illegal access violation) (e.g. see column 3, lines 17 et seq.);

As per claim 4, Lyon discloses in response to TLB/cache miss in which the memory block is not in the local addressable memory, accessing a lower (local) cache within a processor (e.g. see column 1, lines 33-35; column 5, lines 44-46);

As per claim 5, Lyon discloses virtual tag address 207 is received by the virtual CAM 208 for cache access request (e.g. see column 5, lines 44 et seq.);

As per claim 6, Lyon further discloses identifying page address assignment for virtual addresses (e.g. see column 2, lines 8 et seq.; also see column 5, lines 59 et seq.);

As per claim 11, Lyon discloses the invention as claimed

including a method comprises receiving a request (cache access) for access to a memory location by presenting a virtual tag to CAM (e.g. see column 2, lines 49-50; column 5, line 44); identifying a memory block including the memory location (e.g. see column 2, lines 50-52); Lyon further discloses routing the request to one of a local addressable memory and a local cache as being equivalent to the virtual tag 207 are routed and presented to the virtual CAM 208 to generate a virtual TLB hit vector 214 (e.g. see column 5, lines 44 et seq.); Lyon also discloses accessing a local addressable memory (TLB) in response to the TLB hit bit to retrieve physical tag from TLB RAM, the TLB hit bits are then compared to cache tag to determined cache hit or cache miss (e.g. see column 2, line 63 bridging column 3, line 1; also see column 2, lines 52-56) wherein the local addressable memory (TLB) is within the cache which is at the same level of memory as the cache as being claimed (e.g. see figure 3, column 5, lines 28 et seq.);

As per claim 12, Lyon further discloses accessing the local addressable memory (TLB) as being equivalent to the TLB RAM 118 is accessed for retrieving of the physical tag in response to TLB hit or the memory location existing in the local addressable memory (TLB) (e.g. see column 5, lines 10-13);

As per claim 13, generating an illegal access violation exception in response to the memory location not existing in the local addressable memory (TLB) is equivalently taught by Lyon as when there is a TLB MISS condition (memory location is not in

the TLB), the virtual hit vector 214 generates all binary "0s" (illegal access violation) (e.g. see column 3, lines 17 et seq.);

As per claim 15, Lyon discloses the invention as claimed including an apparatus comprising an execution unit is taught as processor known to be embed in the system of Lyon, also being disclosed in the background of Lyon's invention (e.g. see column 1, lines 34 et seq.); an local addressable memory is taught as TLB within a cache memory (e.g. see column 4, lines 22 et seq.), a separate local cache as the same level as the TLC (e.g. see figures 1-3 and column 4, lines 22 et seq.); a local memory controller is known to be embed in the system of Lyon for identifying a memory block including the memory location in response to receiving a request for access to the memory location from the processor (e.g. see column 2, lines 50-52), and routing the request to one of a local addressable memory and a local cache as being equivalent to the virtual tag 207 are routed and presented to the virtual CAM 208 to generate a virtual TLB hit vector 214 (e.g. see column 5, lines 44 et seq.); Lyon also discloses accessing a local addressable memory (TLB) in response to the TLB hit bit to retrieve physical tag from TLB RAM, the TLB hit bits are then compared to cache tag to determined cache hit or cache miss (e.g. see column 2, line 63 bridging column 3, line 1; also see column 2, lines 52-56);

As per claim 16, Lyon discloses a plurality of local memory descriptors as being equivalent to the plurality of TLB hit bits associated with TLB memory blocks (e.g. see column 2, lines 65-

66; column 8, lines 14 et seq.);

As per claim 32; Lyon discloses the invention as claimed including a method comprises receiving a request (cache access) for access to a memory location by presenting a virtual tag to CAM (e.g. see column 2, lines 49-50; column 5, line 44); identifying a memory block including the memory location (e.g. see column 2, lines 50-52); Lyon further discloses examining a local memory descriptor (TLB HIT bit) associated with the memory block (TLB RAM memory block) and accessing a local addressable memory (TLB) in response to the TLB hit bit to retrieve physical tag from TLB RAM, the TLB hit bits are then compared to cache tag to determined cache hit or cache miss (e.g. see column 2, line 63 bridging column 3, line 1; also see column 2, lines 52-56). Lyon discloses in response to TLB/cache miss in which the memory block is not in the local addressable memory, accessing a lower (local) cache within a processor (e.g. see column 1, lines 33-35; column 5, lines 44-46); wherein the local addressable memory (TLB) is within the cache which is at the same memory level as the cache as being claimed (e.g. see figure 3, column 5, lines 28 et seq.);

As per claim 40, Lyon discloses his memory system can be arranged in the hierarchical structure having local cache as L1 cache as being claimed (e.g. see column 1, lines 19 et seq.; also see figures 1-3);

***Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-10, 14, 17-31 and 33-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lyon (USPN: 6,470,437);

As per claim 7; as being detailed above in claim 1, Lyon discloses the local addressable memory is taught as translation lookaside buffer (TLB) (e.g. TLB 114 having TLB RAM 118, e.g. see figure 2; column 5, lines 6 et seq.). Lyon; however, does not particularly discloses the TLB RAM memory being implemented as SRAM type of memory. First of all, it should be noted that SRAM is a commonly-known memory type in the memory storage art; secondly, Applicant neither disclosing in the specification nor claiming in the current invention that different type of cache would change or vary the operation of system. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement Lyon's cache as SRAM type of cache, since SRAM cache is known in the art as cheaper than most other type of memories; in addition, by implementing cache memory as SRAM type, memory refresh is not required, therefore being advantageous.

As per claims 8, 9 and 10; Lyon discloses local memory descriptor (Cacheability/Translation Protection Lookaside Buffer as equivalent to the Translation Lookaside Buffer TLB hit bits are examined and compared to a prevalidated cache tag to determine if a cache hit or cache miss has occurred (e.g. see column 2, line 66 bridging column 3, line 1);

As per claims 14 and 17; as being detailed above in claim 1, Lyon discloses the local addressable memory is taught as translation lookaside buffer (TLB) (e.g. TLB 114 having TLB RAM 118, e.g. see figure 2; column 5, lines 6 et seq.). Lyon; however, does not particularly discloses the TLB RAM memory being implemented as SRAM type of memory. First of all, it should be noted that SRAM is a commonly-known memory type in the memory storage art; secondly, Applicant neither disclosing in the specification nor claiming in the current invention that different type of cache would change or vary the operation of system. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement Lyon's cache as SRAM type of cache, since SRAM cache is known in the art as cheaper than most other type of memories; in addition, by implementing cache memory as SRAM type, memory refresh is not required, therefore being advantageous.

As per claim 18; Lyon discloses local memory descriptor as equivalent to the Translation Lookaside Buffer TLB hit bit for indicating whether an associated memory block resides in the translation lookaside buffer TLB hit/miss (e.g. see column 2,

line 66 bridging column 3, line 1; column 5, lines 44 et seq.);

As per claim 19, Lyon discloses the invention as claimed including an apparatus comprising an execution unit is taught as processor known to be embed in the system of Lyon, also being disclosed in the background of Lyon's invention (e.g. see column 1, lines 34 et seq.); an local addressable memory is taught as TLB within a cache memory (e.g. see column 4, lines 22 et seq.), a separate local cache as the same level as the TLC (e.g. see figures 1-3 and column 4, lines 22 et seq.); a local memory controller is known to be embed in the system of Lyon for identifying a memory block including the memory location in response to receiving a request for access to the memory location from the processor (e.g. see column 2, lines 50-52), and routing the request to one of a local addressable memory and a local cache as being equivalent to the virtual tag 207 are routed and presented to the virtual CAM 208 to generate a virtual TLB hit vector 214 (e.g. see column 5, lines 44 et seq.); Lyon also discloses accessing a local addressable memory (TLB) in response to the TLB hit bit to retrieve physical tag from TLB RAM, the TLB hit bits are then compared to cache tag to determined cache hit or cache miss (e.g. see column 2, line 63 bridging column 3, line 1; also see column 2, lines 52-56), a system bus coupled to the processor and different interface unit is known to be embedded in the system of Lyon (e.g. see figures 1-4). Lyon discloses the invention as claimed except for the system comprises a universal serial Bus interface. First of all, USB interface is notorious

old and well known in the art for its ability to support plug and play operation, allowing easy installation of peripherals and faster data transfer rate. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention as made to implement an USB interface in the system of Lyon in order to arrive at Applicant's current invention. In doing so, it would allow the system of Lyon to serve broader range of applications, and to provide Lyon's system the ability (a) to simplify connection of external devices, and (b) to support plug and play operation, therefore being advantageous.

As per claim 20, Lyon discloses the local addressable memory is taught as translation lookaside buffer (TLB) (e.g. TLB 114 having TLB RAM 118, e.g. see figure 2; column 5, lines 6 et seq.). Lyon; however, does not particularly discloses the TLB RAM memory being implemented as SRAM type of memory. First of all, it should be noted that SRAM is a commonly-known memory type in the memory storage art; secondly, Applicant neither disclosing in the specification nor claiming in the current invention that different type of cache would change or vary the operation of system. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement Lyon's cache as SRAM type of cache, since SRAM cache is known in the art as cheaper than most other type of memories; in addition, by implementing cache memory as SRAM type, memory refresh is not required, therefore being advantageous.

As per claims 21-24 and 25-27; Lyon discloses the invention as claimed, detailed above with respect to claims 1-10 and 11-14; Lyon however does not particularly disclose a computer-readable medium of instructions to be implemented on a computer as being claimed in claims 21-24 and 25-27. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the software onto another system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Lyon's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Lyon's program on other systems.

As per claim 28, Lyon discloses the invention as claimed including a method comprises accessing a local memory (translation lookaside buffer, TLB; e.g. see column 5, lines 44 et seq.), Lyon further discloses the local memory (TLB) is within the cache which is at the same memory level as the cache wherein the local memory is considered an extension of local memory address space (e.g. see figure 3, column 5, lines 28 et seq.). Lyon discloses the invention as claimed except for configuring

the local memory as SDRAM. First of all, it should be noted that SRAM is a commonly-known memory type in the memory storage art; secondly, Applicant neither disclosing in the specification nor claiming in the current invention that different type of cache would change or vary the operation of system. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement Lyon's cache as SRAM type of cache, since SRAM cache is known in the art as cheaper than most other type of memories; in addition, by implementing cache memory as SRAM type, memory refresh is not required, therefore being advantageous.

As per claim 29, Lyon discloses by setting the TLB hit bit to "1" indicating the location of the virtual tag 207 in the virtual CAM (extending the local virtual memory space) (e.g. see column 5, lines 47-49);

As per claims 30 and 31; Lyon discloses the invention as claimed, detailed above with respect to claims 28-29. Lyon however does not particularly disclose a computer-readable medium of instructions to be implemented on a computer as being claimed in claims 21-24 and 25-27. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is generally well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from

which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the software onto another system. The examiner takes Official Notice of this teaching. Therefore, it would have been obvious to put Lyon's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Lyon's program on other systems.

As per claims 33-39, Lyon discloses his memory system can be arranged in the hierarchical structure having local cache as L1 cache as being claimed (e.g. see column 1, lines 19 et seq.; also see figures 1-3);

*Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval

(PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***TVT***/January 18, 2005

***Tuan V. Thai***
**PRIMARY EXAMINER**
**Group 2100**